EUV – Supporting Moore's Law

Marcel Kemp
Director Investor Relations - Europe

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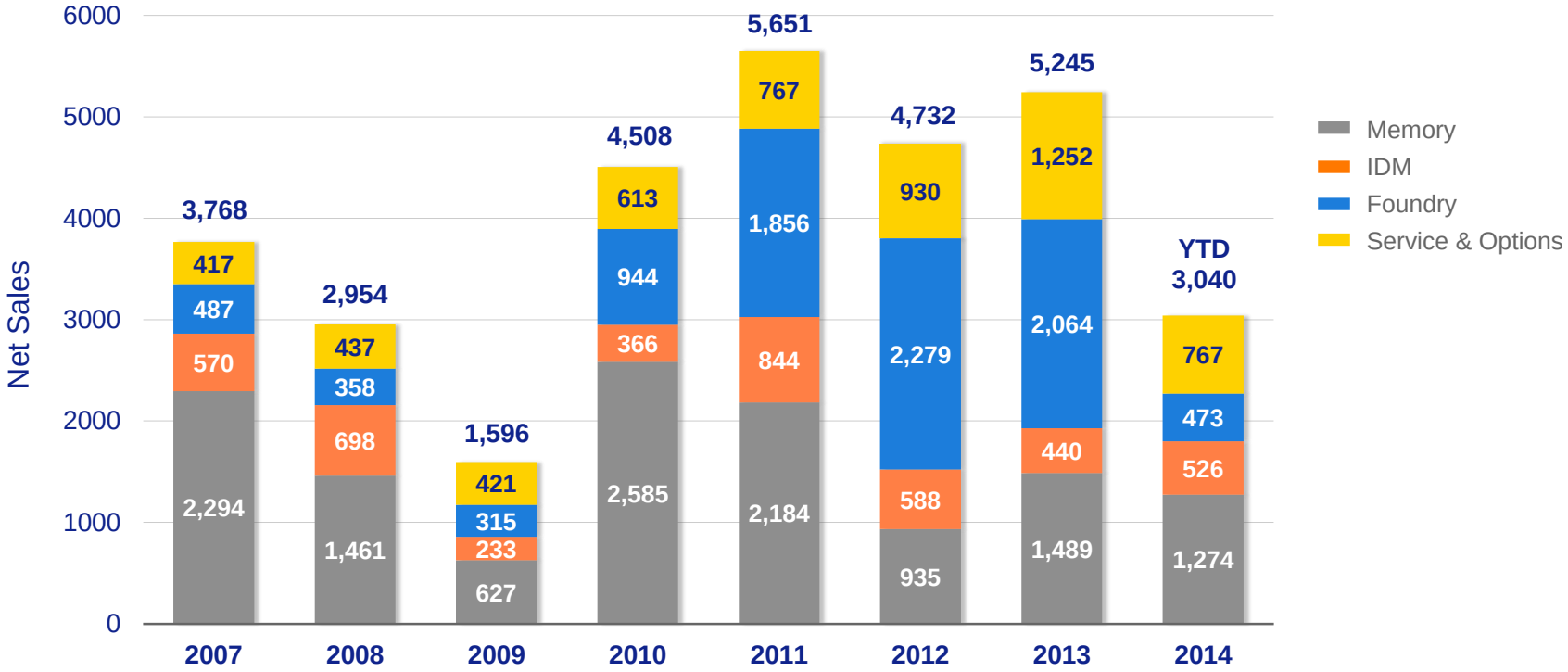
Forward looking statements

This document contains statements relating to certain projections and business trends that are forward-looking, including statements with respect to our outlook, expected customer demand in specified market segments, expected sales levels, systems backlog, IC unit demand, expected financial results, gross margin and expenses, expected shipment of tools, productivity of our tools, the development of EUV technology and the number of EUV systems expected to be shipped and timing of shipments, dividend policy and intention to repurchase shares. You can generally identify these statements by the use of words like “may”, “will”, “could”, “should”, “project”, “believe”, “anticipate”, “expect”, “plan”, “estimate”, “forecast”, “potential”, “intend”, “continue” and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve risks and uncertainties. Actual results may differ materially from projected results as a result of certain risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), including the impact of general economic conditions on consumer confidence and demand for our customers’ products, competitive products and pricing, the impact of manufacturing efficiencies and capacity constraints, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products, the number and timing of EUV systems expected to be shipped, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, availability of raw materials and critical manufacturing equipment, trade environment, changes in exchange rates, available cash, distributable reserves for dividend payments and share repurchases, and other risks indicated in the risk factors included in ASML’s Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

Content

- Semiconductor environment
- Challenges of shrink
- Our response: the lithography roadmap

Total net sales M€ by End-use



Numbers have been rounded for readers' convenience

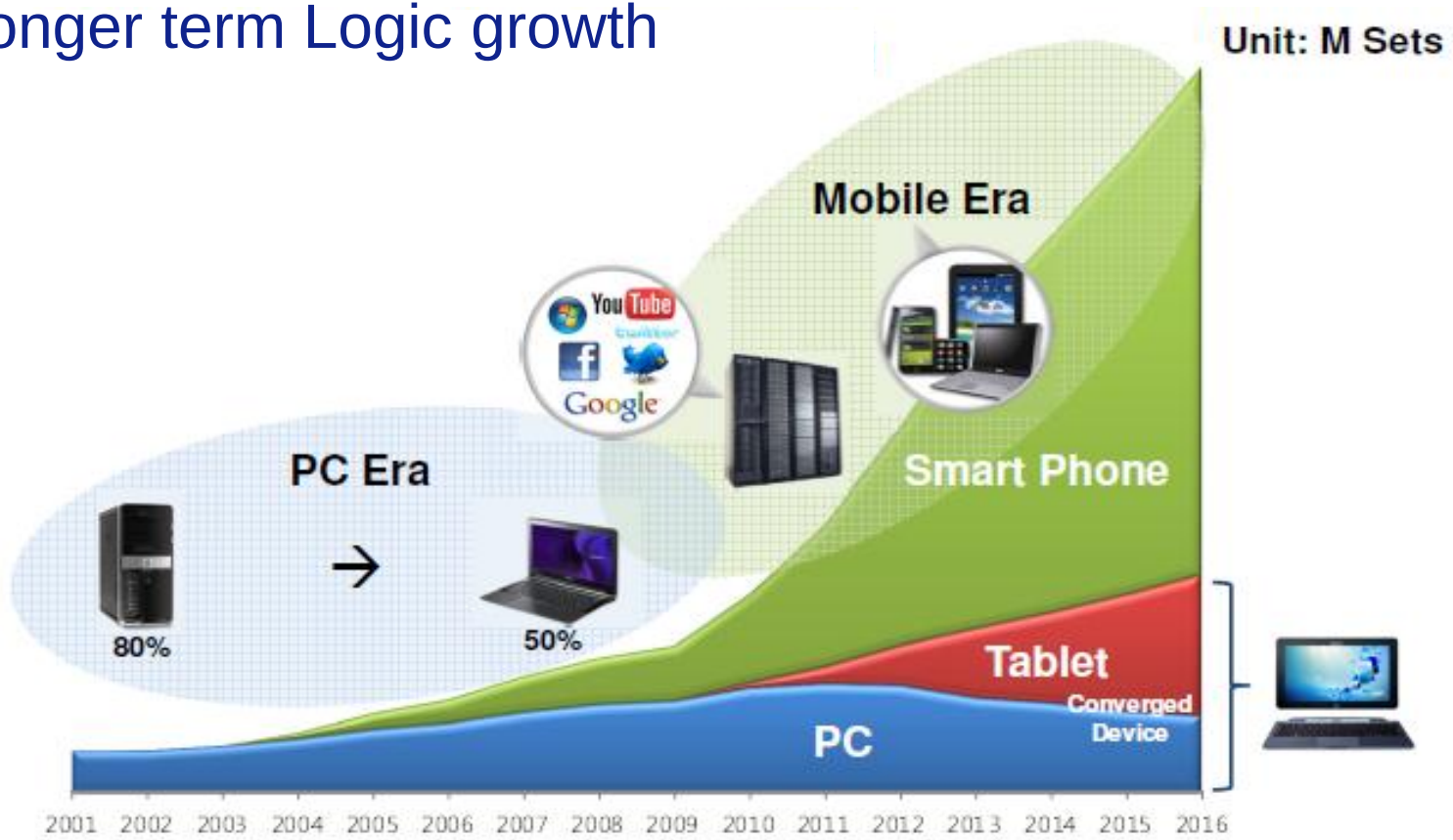
Business environment

- The ramp of the 20/16/14 nm nodes is set to continue, however as we discussed last quarter some customers continue to evaluate the timing of their litho deliveries to synchronize supply and demand, leading to an adjustment of the ASML Q4 shipment forecast
- Expected total installed 20/16/14 nm to reach a capacity of approx. 300,000 wspm (wafer starts/month)

- Bit growth forecast low 40s%
- Demand being met through planar NAND shrink and capacity expansion
- No Vertical NAND capacity being added in H2 2014

- Bit growth forecast of 20 - 30%
- Bits supplied by planned technology transitions meet bit demand forecast
- Litho process intensity increases due to node transition and mobile DRAM process complexity

The rise of smart phones and tablets → Longer term Logic growth

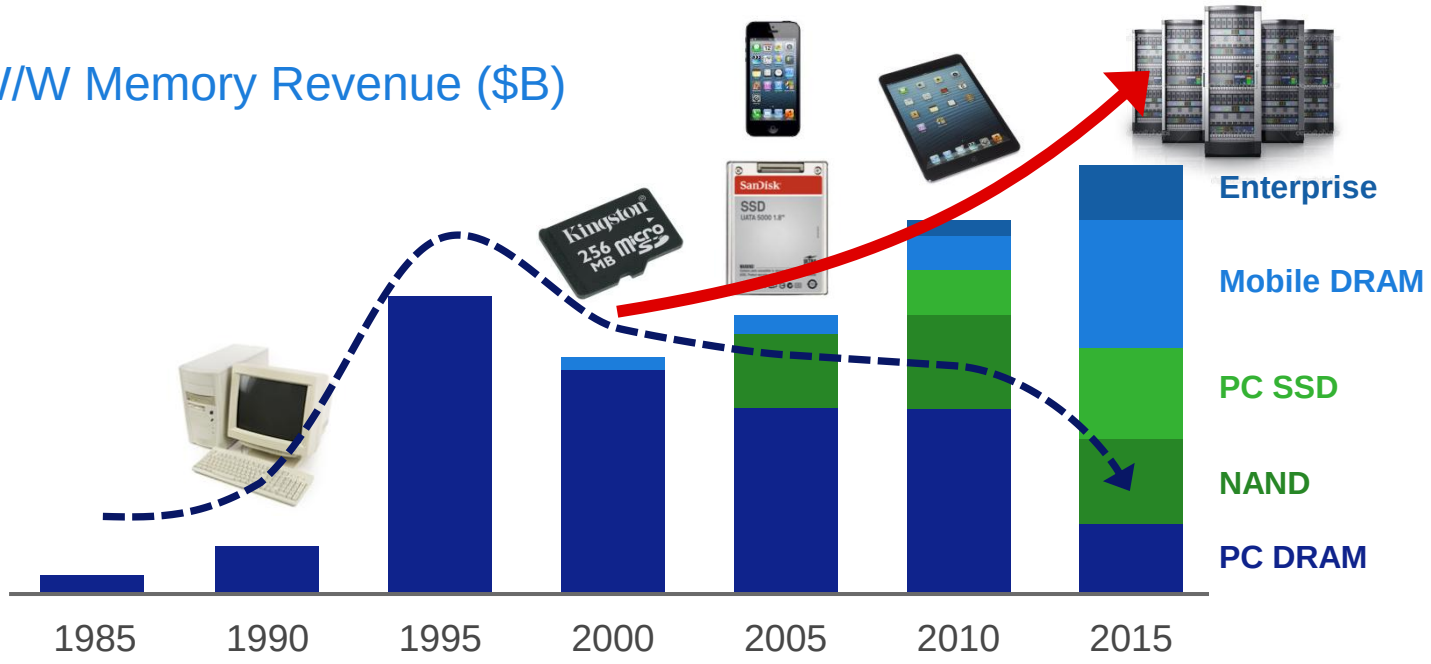


Source:
Pablo Temprano,
Samsung, ISS
Jan 2014

Product trends and memory market evolution → Memory growth

PC → Mobile → Big Data

W/W Memory Revenue ($B)



Source:
Pablo Temprano, Samsung
ISS, Jan 2014

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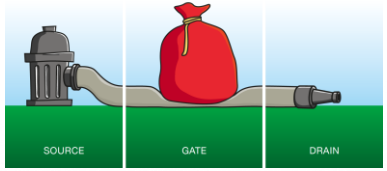
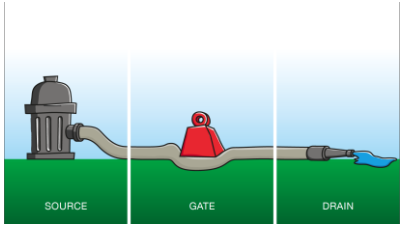
No end in sight for logic scaling

Bulk CMOS:100nm gate length



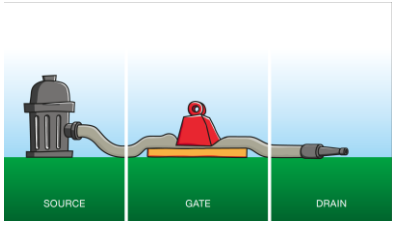
N20

Bulk CMOS:
Complementary Metal Oxide Semiconductor



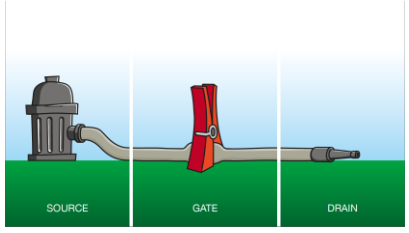
N20 / N14

SOI:
Silicon on Insulator



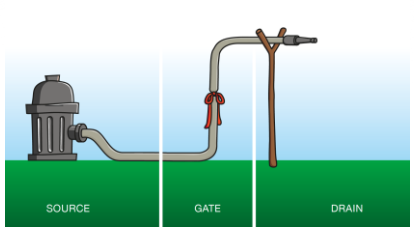
N1x / N7

Bulk FinFet :
Fin field effect transistor



N7 / N5

SOI FinFet :
Silicon on insulator fin field effect transistor, III-V



N5 / N3.5

Gate-all-around transistor

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Our Challenge: enable affordable scaling

- Scaling needs to create **lower cost and improved performance – ie., support Moore's Law**
- Affordable scaling in lithography can be achieved:
  - In the near term **- Immersion**: drive **productivity and yield (overlay and focus control)** with multiple patterning using advanced litho equipment extended with application products - Holistic Lithography/Yieldstar
  - In the mid/long term **- EUV:** drive **productivity/availability** and improve **operational cost**

Affordable shrink roadmap

2012 2013 2014 2015 2016 2017 2018 2019 2020

Immersion

OVERL[illegible] m

THR[illegible] 50 wph

EUV

7 nm

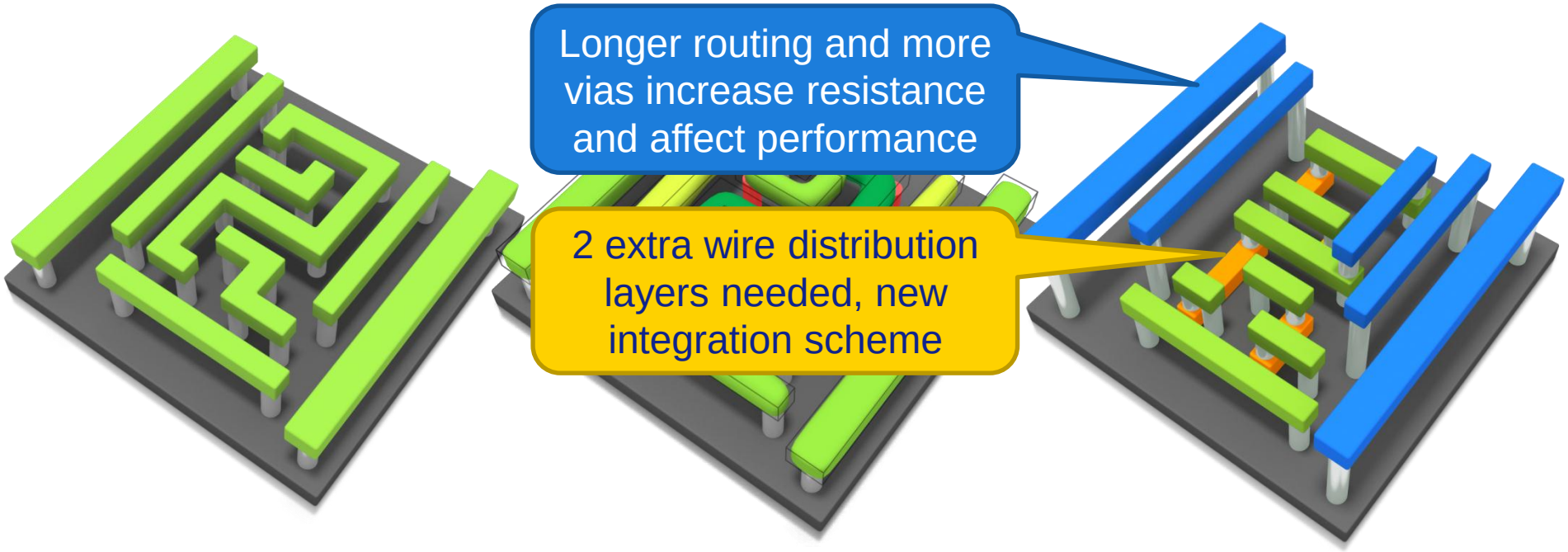
ArF Dry
KrF

Overla[illegible] 1460K system
[illegible] system)
Extend the productivity [illegible] critical KrF (XT:860L/800-3D): memory applications

Supported by a Holistic Lithography approach using computational litho, overlay and CD metrology, feedback loops for wider process window creation and process control

Today immersion extensions at 10 nm node possible with 1D

But critical metal layers require extra wiring layers, adding processing complexity and cost; decreasing chip performance

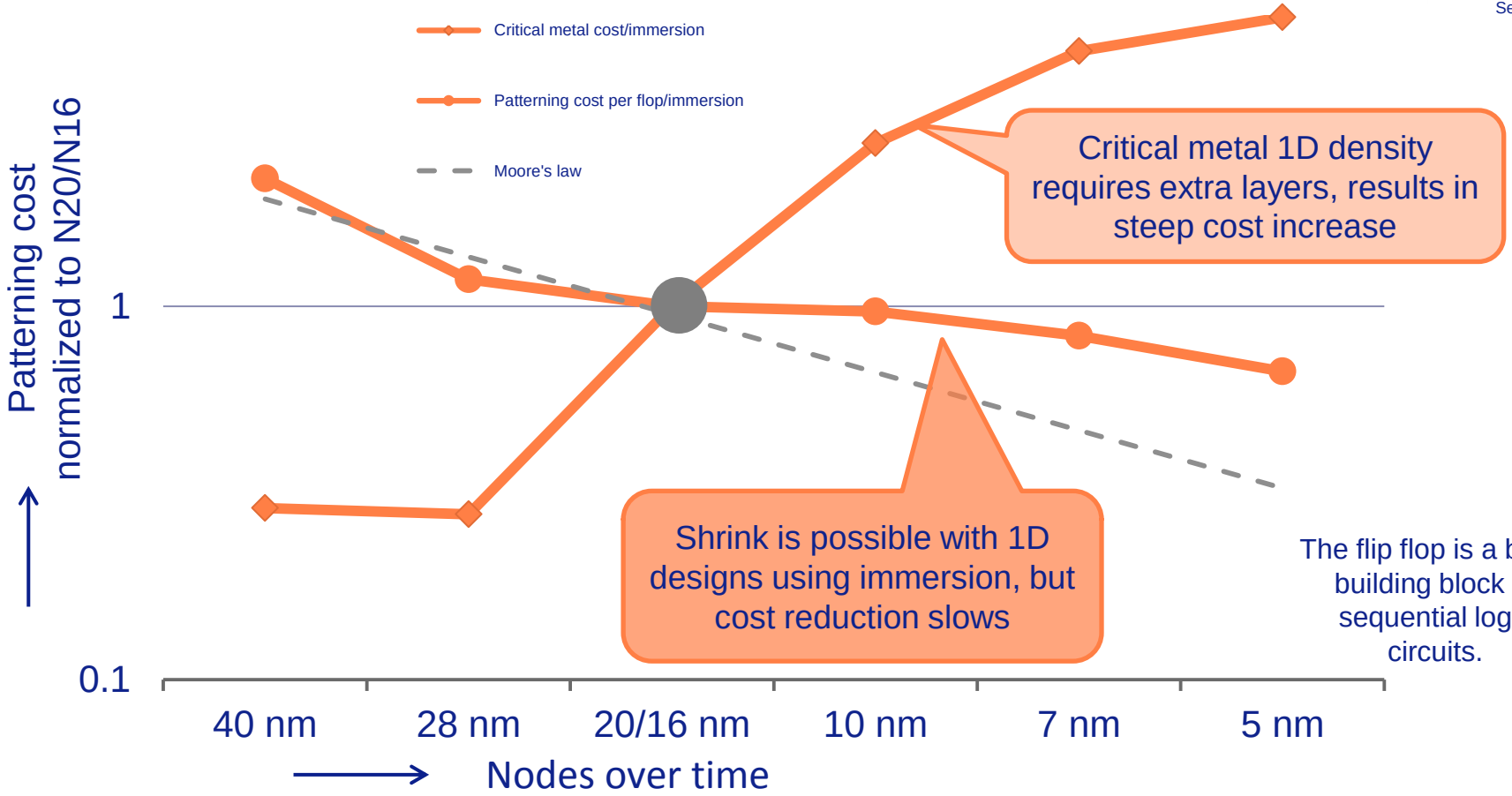


EUV 2D metal structure
Single layer solution

ArFi 2D metal structure
3-4 exposures, single layer
insufficient patterning fidelity

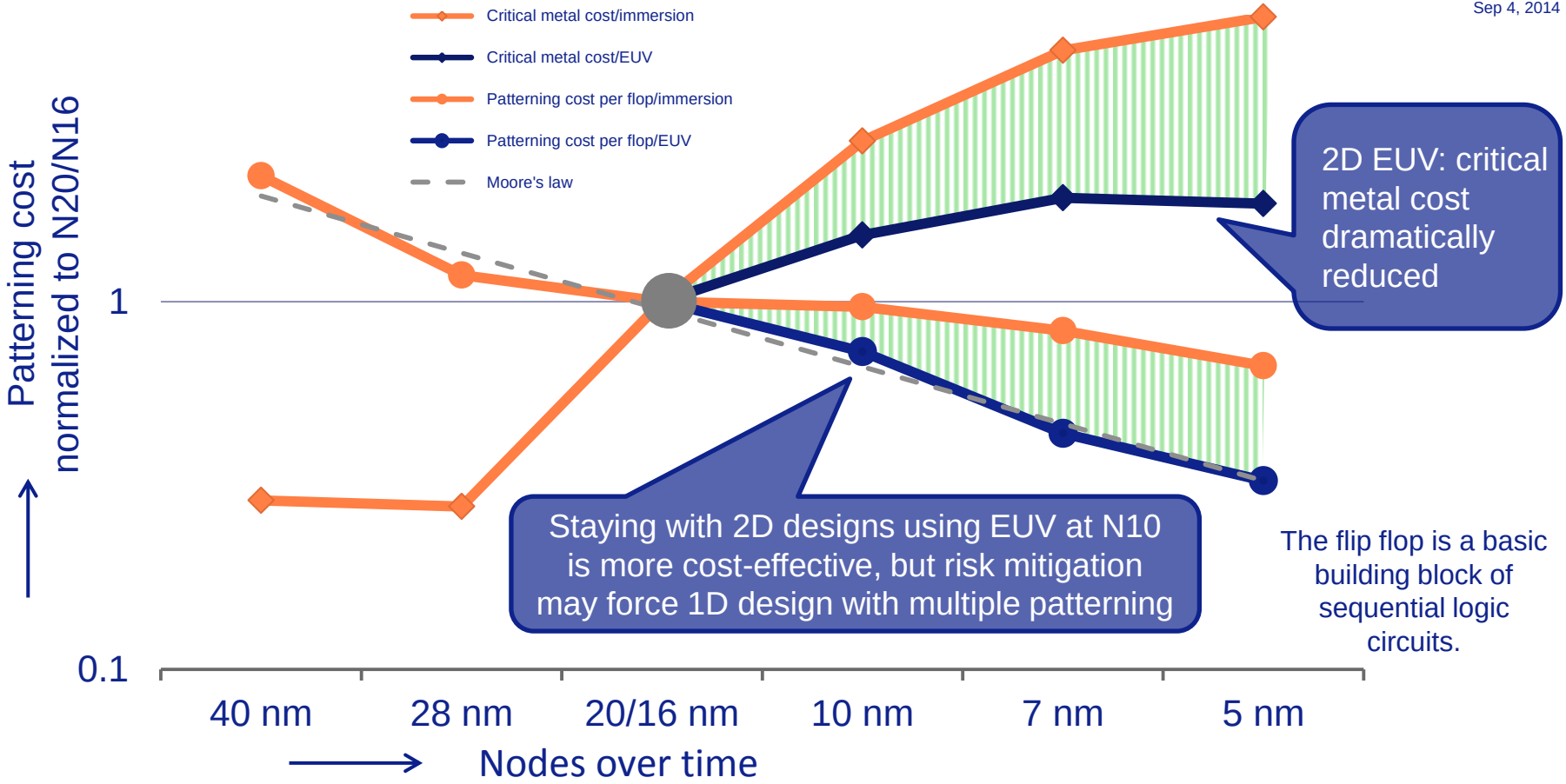
ArFi 1D metal structure
6-9 exposures in 3 layers

Cost: 1D/immersion vs 2D/EUV



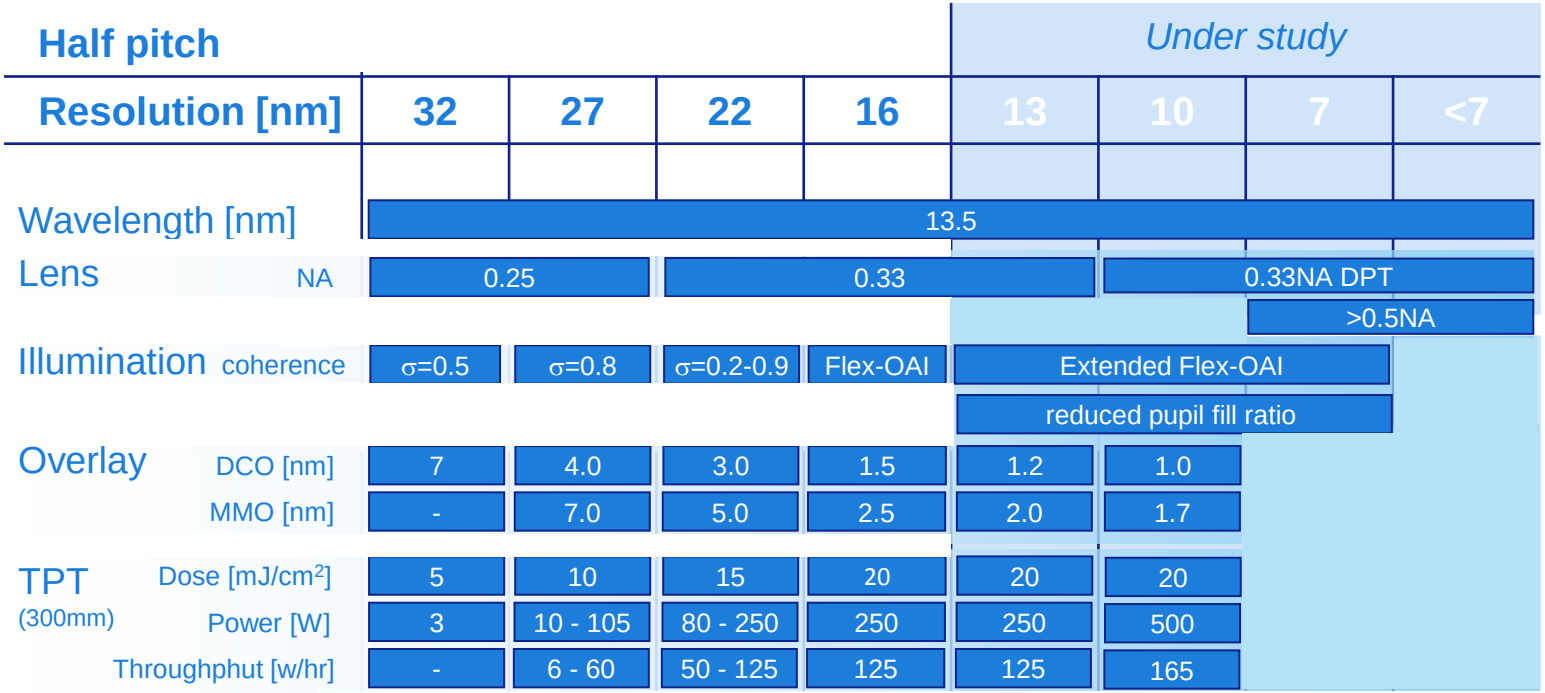
The flip flop is a basic building block of sequential logic circuits.

Cost: 1D/immersion vs 2D/EUV

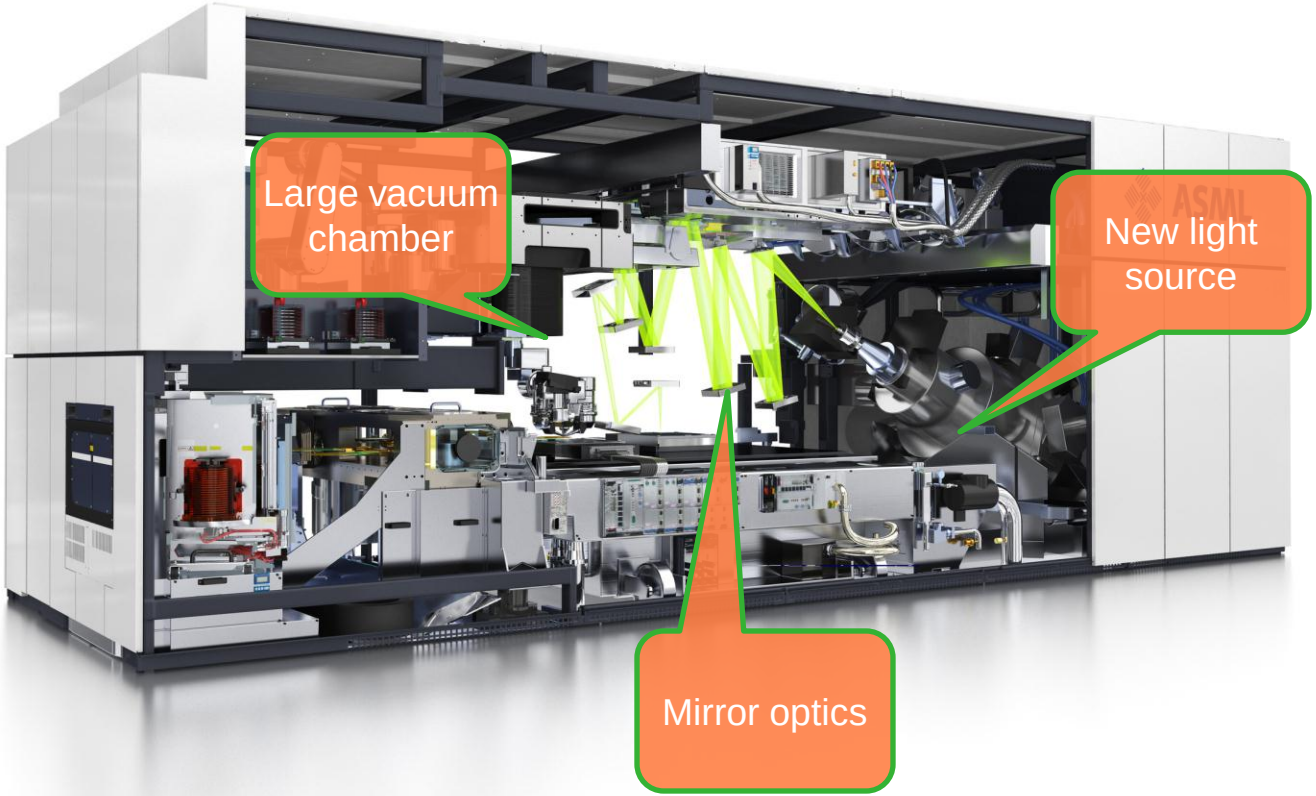


The flip flop is a basic building block of sequential logic circuits.

EUV technology roadmap - extendibility to <7nm (half pitch) → > 5x node generations

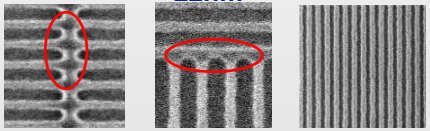


EUV: Evaluations for 10nm process insertion underway

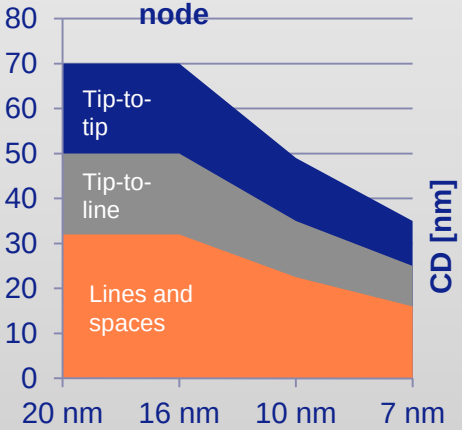


What did we achieve since last year?

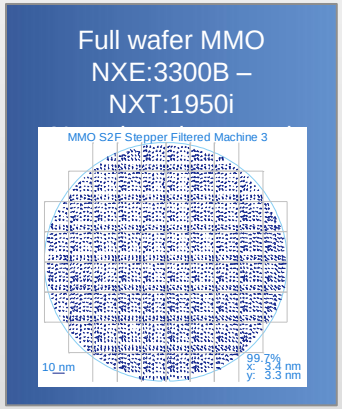
EUV meets aggressive 2D logic imaging requirements

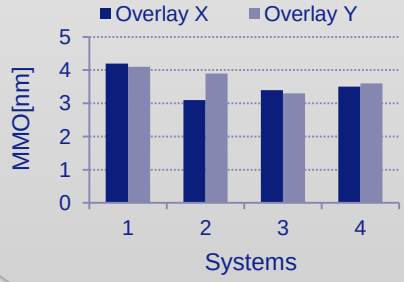


CD requirements by node



Good Matched Machine Overlay performance

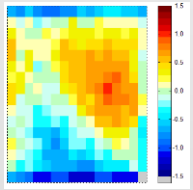


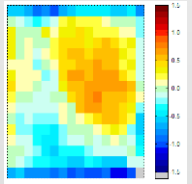


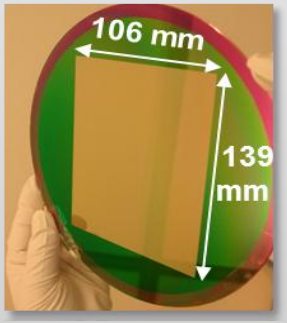
Full size free-standing pSi proto-type pellicle realized

Without pellicle
CD map (nominal energy) Center field 27 nm L&S

With pellicle
CD map (nominal energy) Center field 27 nm L&S



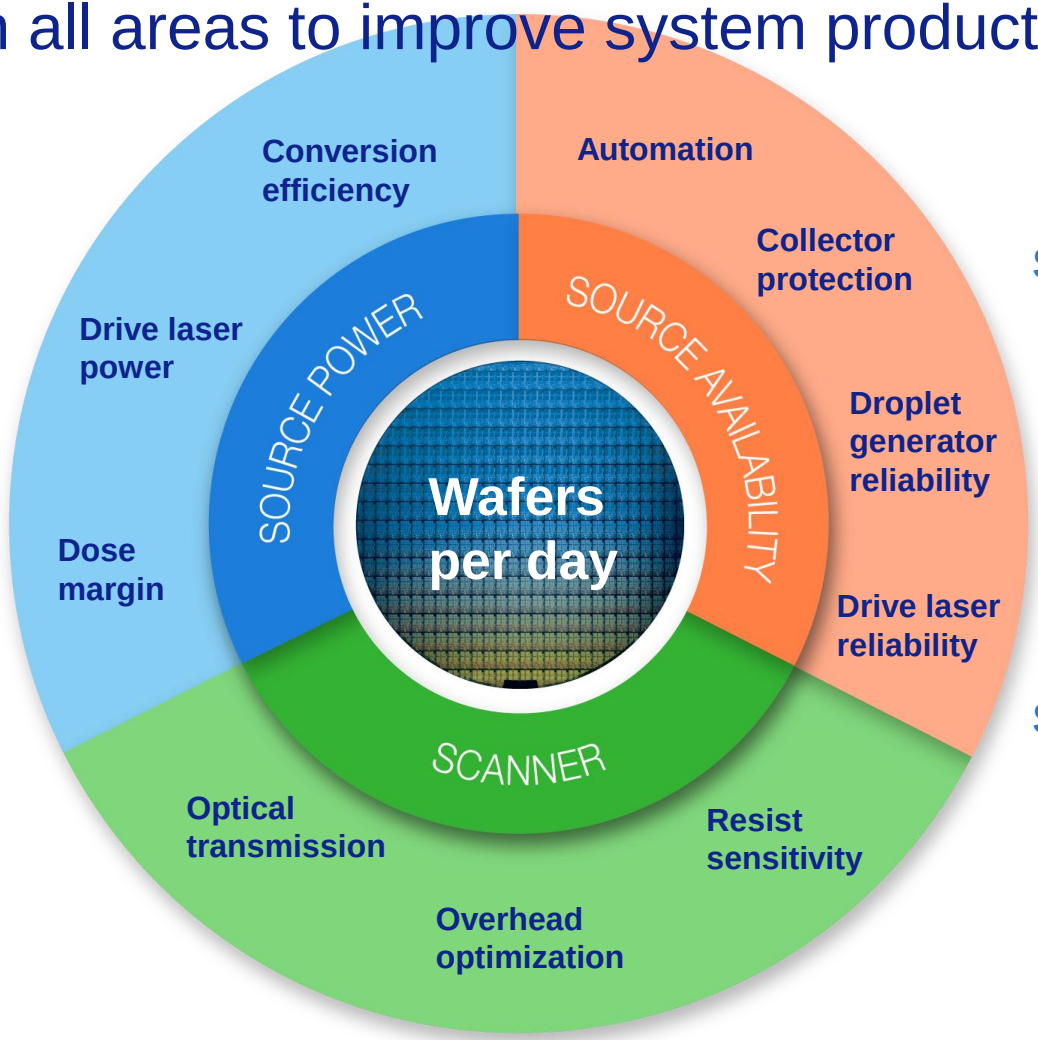




Progress on all areas to improve system productivity

Source Power

- Higher conversion efficiency demonstrated
- Advanced dose controller demonstrated



System Availability

- Full automation plasma control with good dose control demonstrated
- In-situ cleaning of collector demonstrated

Scanner

- Improved coatings for better transmission
- Reduced overhead ongoing

EUV status at customers: Towards production insertion

For process development, customers typically require 100 wafers per day.

For pre-production customers have asked us to deliver 500 wafers per day by the end of 2014.

- 2014 Q1 : 100 wafers per day √
- Q2 : 200 wafers per day √
- Q4 : 500 wafers per day
- In 2016 we will provide our customers with the productivity needed for volume production (typically up to 1,500 wafers/day)

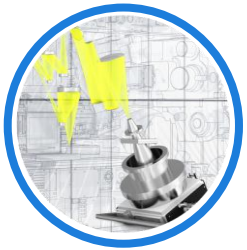
- 6 NXE:3300B systems fully qualified and shipped to customers
- 5 more NXE:3300B systems being integrated (3x upgrades NXE:3300B → NXE:3350B)
- 4th generation NXE system (NXE:3350B) integration ongoing
- EUV cleanroom extension is under construction

Summary : EUV towards production insertion

Multiple customers are qualifying EUV for insertion at the N10 nm logic node

Imaging and overlay is in line with requirements for N10 insertion

Defect reduction ~10x per year shown and full-size EUV pellicle prototype manufactured



EUV source: Improvements demonstrated in conversion efficiency, dose margin, automation and collector lifetime, driving power and availability

- The value of EUV is undisputed as the lithographic shrink technology of choice for multiple nodes starting in 2016/2017.
- Our customers and peers continue to support and drive development of EUV systems and infrastructure for introduction of EUV into volume production in the stated timeframe.

ASML